

[voltage limiter] internal power supply means provided on said chip for reducing an external supply voltage to an internal supply voltage lower than said external supply voltage within said chip;

wherein, when said external supply voltage is not higher than a predetermined first voltage, the internal supply voltage of said [voltage limiter] internal power supply means increases at a first rate which is substantially equal to the increasing rate of said external supply voltage, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage increases at a second rate which is lower than the increasing rate of said external supply voltage, and after said external supply voltage exceeds said second voltage, said internal supply voltage increases at a third rate which is higher than the second rate, wherein said first circuits are fed said internal supply voltage, said [first circuits are] internal power supply means is fed a control signal and wherein a driving ability of said [voltage limiter] internal power supply means is controlled by said control signal.

Sub G 3
13. (three times amended) A semiconductor integrated circuit comprising:

a chip;
load circuits provided on said chip; and
[voltage limiter] internal power supply means provided on said chip for reducing an external supply voltage to an

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internal supply voltage lower than said external supply voltage within said chip and supplying it to said load circuits;

wherein said load circuits are fed said internal supply voltage, said [load circuits are] internal power supply means is fed a control signal and wherein a driving ability of said [voltage limiter] internal power supply means is controlled by said control signal.

Claim 15, line 3, delete "voltage limiter" and insert --
internal power supply --.

Claim 16, line 4, delete "voltage limiter" and insert --
internal power supply --.

Please add new claims 20-73 as follows:

20. A semiconductor integrated circuit comprising;
a chip;
a first circuit provided on said chip;
a second circuit provided on said chip;
an internal power supply means, provided on said chip,
for supplying an internal supply voltage which is lower than an
external supply voltage;

a reference voltage generating means, provided on said
chip, for generating a reference voltage;
wherein said reference voltage provided by said
reference voltage generating means is fed to said internal power
supply means, said internal supply voltage provided by said

internal power supply means is fed to said second circuit, and
said external supply voltage is fed to said first circuit.

21. A semiconductor integrated circuit comprising;
a chip;
a first circuit provided on said chip;
a second circuit provided on said chip;
an internal power supply means, provided on said chip,
for supplying an internal supply voltage which is lower than an
external supply voltage;
a reference voltage generating means, provided on said
chip, for generating a reference voltage;
wherein said reference voltage provided by said
reference voltage generating means is fed to said internal power
supply means, said internal supply voltage provided by said
internal power supply means is fed to said second circuit, said
external supply voltage is fed to said first circuit, and a
breakdown voltage of a first transistor having fed thereto said
external supply voltage is higher than a breakdown voltage of a
second transistor having fed thereto said internal supply
voltage.

22. A semiconductor integrated circuit comprising;
a substrate;
a first circuit, provided on said substrate, having a
first transistor;

a second circuit, provided on said substrate, having a second transistor;

an internal power supply means, provided on said substrate, for supplying an internal supply voltage which is lower than an external supply voltage;

a reference voltage generating means, provided on said substrate, for generating a reference voltage;

wherein said internal supply voltage provided by said internal power supply means is fed to said second circuit, said external supply voltage is fed to said first circuit and said internal power supply means includes a converter transistor which outputs said internal supply voltage, said converter transistor having a control electrode; and

wherein said internal supply voltage is controlled by said reference voltage supplied to said control electrode of said converter transistor.

23. A semiconductor integrated circuit comprising:

a chip;

an external supply voltage, provided on said chip, for receiving an external supply voltage;

an interface circuit provided on the chip;

an internal circuit on the chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is lower than said external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage;

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, said internal supply voltage provided by said internal power supply means is fed to said internal circuit and said external supply voltage is fed to said interface circuit.

24. A semiconductor integrated circuit comprising;

a chip;

load circuits provided on said chip; and

internal power supply means provided on said chip for changing an external supply voltage to an internal supply voltage lower than said external supply voltage within said chip and supplying it to said load circuits;

wherein said load circuits are fed said internal supply voltage, said internal power supply means is fed a control signal and wherein a driving ability of said internal power supply means is changed according to an operation of the load.

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25. The semiconductor integrated circuit according to claim 11, wherein said reference voltage is a voltage other than ground potential.

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26. The semiconductor integrated circuit according to claim 11, wherein said reference voltage generating means comprises:
a resistor.

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27. The semiconductor integrated circuit according to claim
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20, wherein said reference voltage generating means comprises:
a *third* transistor.

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28. The semiconductor integrated circuit according to claim
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27, wherein said *third* transistor receives a control signal.

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29. The semiconductor integrated circuit according to claim
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30, wherein said reference voltage generating means comprises:
a *third* transistor and a resistor.

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30. The semiconductor integrated circuit according to claim
29, wherein said *third* transistor receives a control signal.

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31. The semiconductor integrated circuit according to claim
30, wherein said second circuit comprises:
a plurality of memory cells.

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32. The semiconductor integrated circuit according to claim
31, wherein said first transistor of said reference voltage
generating means is an gate field effect transistor.

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33. The semiconductor integrated circuit according to claim
28, wherein said first transistor of said reference voltage
generating means is an gate field effect transistor.

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- 24* 34. The semiconductor integrated circuit according to claim
21, wherein said reference voltage is a voltage other than ground potential.
- 24* 35. The semiconductor integrated circuit according to claim
21, wherein said reference voltage generating means comprises:
a resistor.
- 24* 36. The semiconductor integrated circuit according to claim
21, wherein said reference voltage generating means comprises:
a third transistor.
- 27* 37. The semiconductor integrated circuit according to claim
36, wherein said third transistor receives a control signal.
- 24* 38. The semiconductor integrated circuit according to claim
21, wherein said reference voltage generating means comprises:
a third transistor and a resistor.
- 31* 39. The semiconductor integrated circuit according to claim
38, wherein said third transistor receives a control signal.
- 32* 40. The semiconductor integrated circuit according to claim
39, wherein said second circuit comprises:
a plurality of memory cells.

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41. The semiconductor integrated circuit according to claim
³⁴ 40, wherein said first, second and third transistors are
insulated gate field effect transistors.

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42. The semiconductor integrated circuit according to claim
³⁷, wherein said first, second and third transistors are
insulated gate field effect transistors.

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43. The semiconductor integrated circuit according to claim
²², wherein said reference voltage is a voltage other than
ground potential.

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44. The semiconductor integrated circuit according to claim
²², wherein said reference voltage generating means comprises:
a resistor.

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45. The semiconductor integrated circuit according to claim
²², wherein said reference voltage generating means comprises:
a third transistor.

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46. The semiconductor integrated circuit according to claim
⁴⁵, wherein said third transistor receives a control signal.

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47. The semiconductor integrated circuit according to claim
²², wherein said reference voltage generating means comprises:
a third transistor and a resistor.

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⁴³ 48. The semiconductor integrated circuit according to claim
⁴⁷, wherein said third transistor receives a control signal.

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⁴⁸ 49. The semiconductor integrated circuit according to claim
wherein said second circuit comprises:
a plurality of memory cells.

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⁴⁹ 50. The semiconductor integrated circuit according to claim
49, wherein said first, second and third transistors are
insulated gate field effect transistors.

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⁴⁹ 51. The semiconductor integrated circuit according to claim
46, wherein said first, second and third transistors are
insulated gate field effect transistors.

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⁵² 52. The semiconductor integrated circuit according to claim
23, wherein said reference voltage is a voltage other than ground
potential.

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⁵³ 53. The semiconductor integrated circuit according to claim
23, wherein said reference voltage generating means comprises:
a resistor.

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⁵⁴ 54. The semiconductor integrated circuit according to claim
23, wherein said reference voltage generating means comprises:
a third transistor.

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55. The semiconductor integrated circuit according to claim
52, wherein said third transistor receives a control signal.

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56. The semiconductor integrated circuit according to claim
48, wherein said reference voltage generating means comprises:
a third transistor and a resistor.

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57. The semiconductor integrated circuit according to claim
56, wherein said third transistor receives a control signal.

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58. The semiconductor integrated circuit according to claim
57, wherein said second circuit comprises:
a plurality of memory cells.

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59. The semiconductor integrated circuit according to claim
58, wherein said first, second and third transistors are
insulated gate field effect transistors.

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60. The semiconductor integrated circuit according to claim
55, wherein said first, second and third transistors are
insulated gate field effect transistors.

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61. A semiconductor integrated circuit according to claim
28, wherein said ~~first~~^{third} transistor is fed said control signal to
control an operation of said first transistor.

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20 62. The semiconductor integrated circuit according to claim
30, wherein said *first* transistor is fed said control signal to
control an operation of said first transistor.

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28 63. The semiconductor integrated circuit according to claim
37, wherein said third transistor is fed said control signal to
control an operation of said third transistor.

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32 64. The semiconductor integrated circuit according to claim
39, wherein said third transistor is fed said control signal to
control an operation of said third transistor.

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40 65. The semiconductor integrated circuit according to claim
46, wherein said third transistor is fed said control signal to
control an operation of said third transistor.

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44 66. The semiconductor integrated circuit according to claim
48, wherein said third transistor is fed said control signal to
control an operation of said third transistor.

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53 67. The semiconductor integrated circuit according to claim
55, wherein said third transistor is fed said control signal to
control an operation of said third transistor.

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57 68. The semiconductor integrated circuit according to claim
57, wherein said third transistor is fed said control signal so
as to control an operation of said third transistor.

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69. The semiconductor integrated circuit according to claim
¹¹ 20, wherein a breakdown voltage of a first transistor of said
first circuit is higher than a breakdown voltage of a second
transistor of said second circuit.

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⁴⁸ 70. The semiconductor integrated circuit according to claim
23, wherein a breakdown voltage of a first transistor of said
interface circuit is higher than a breakdown voltage of a second
transistor of said internal circuit.

71. The semiconductor integrated circuit according to claim
7, wherein a load capacitance of said first circuits is changed
by said control signal.

72. The semiconductor integrated circuit according to claim
13, wherein a load capacitance of said load circuits is changed
by said control signal.

73. The semiconductor integrated circuit according to claim
16, wherein a load capacitance of said load circuits is changed
by said control signal. *74*

REMARKS

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